MT7981B Datasheet

Version: 1.3
Release date: 2023-03-22

Overview

MT7981B is a highly integrated wireless network router system-on-chip used for high wireless performance, home entertainment, and home automation and so on.

Applications:
- Internet Service Router
- Wireless Router
- Wireless Repeater
- Home Security Gateway
- Home Automation
- NAS Devices

MT7981B is fabricated with advanced silicon process and integrates a Dual-core ARM® Cortex-A53 MPCoreTM operating up to 1.3GHz and more DRAM bandwidth. This SoC also includes a variety of peripherals, including SGMII, and USB3.0 (Host) ports. To support popular network applications, MT7981B also implements two 2.5Gbps HSGMII Ethernet interface. MT7981B combines with a RF chip, they can provide dual-band concurrent chipset solution for WIFI6 AX3000 wireless router platform.

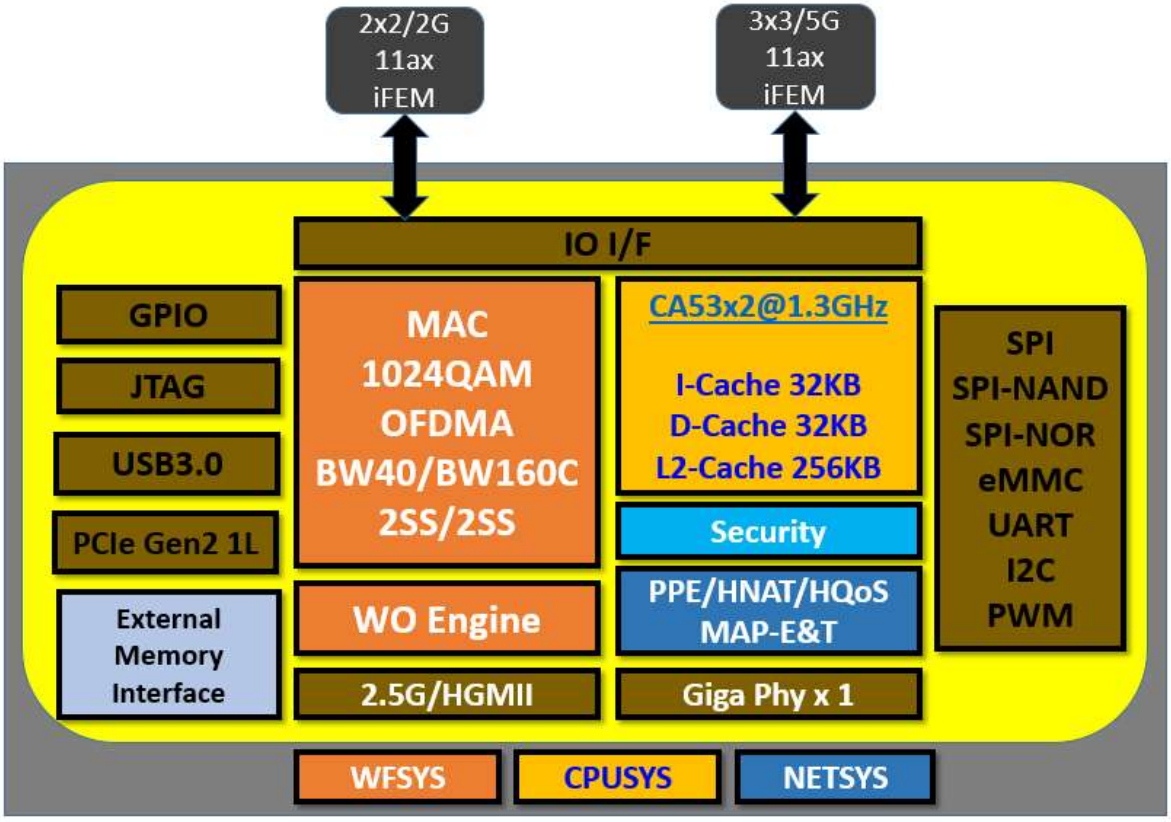
Besides the connectivity features, the hardware-based NAT engine with QoS embedded in MT7981B transporting the audio/video streams in higher priority than other non-timely services also enriches the home entertainment application. The SFQ separating P2P sessions from audio/video ones so that MT7981B guarantees the streaming service.

With the advanced technology and abundant features, MT7981B is well positioned to be the core of next-generation Smart WiFi AP router, and home gateway systems.

Key Features

- Embedded dual-core ARM® Cortex-A53 MPCore operating at 1.3GHz
  - 32KB L1 I-Cache and 32KB L1 D-Cache
  - 256KB unified L2 Cache
  - NEON/FPU
- External memory interface
  - Support DDR3/DDR4-2133 2GB
- NOR (SPI), NAND Flash (SPI, SLC), eMMC4.5/SD
- USB3.0 Host x 1
- SPI, I2C, UART Lite, JTAG, MDC, MDIO, GPIO, PWM, I2S
- Two HSGMII(2.5Gbps) interfaces
- Giga Bit Ethernet
  - 1-port 10/100/1000Mbps MDI transceivers
- WiFi
  - Lead in 2x2+3x3 WIFI6 integration
  - Airtime Fairness
  - Spectrum Analyzer
- HW NAT
  - Etherent/WiFi
  - Wired speed
  - IPv4 routing, NAT, NAPT
  - IPv6 routing, DS-Lite, 6RD, 464XLAT, MAP-E/T
- HW QoS
  - 64 hardware queues to guarantee the min/max bandwidth of each flow.
  - Seamlessly co-work with HW NAT engine.
  - SFQ w/ 1k queues.
- Security
  - Secure boot
  - Crypto engine (EIP97)
- Green
  - Intelligent Clock Scaling (exclusive)
  - DDR: ODT off, Self-refresh mode

Functional Block Diagram



Document Revision History

Revision	Date	Author	Description
0.1	2021-11-01	Yi-Tao.Tsai	Initial Release
0.2	2021-12-23	Yi-Tao.Tsai	Fix Table 2-2 pin description
0.3	2022-03-09	Yi-Tao.Tsai	Fix Top marking: MT7981B → MT7981BA
0.4	2022-03-23	Yi-Tao.Tsai	Fix Top marking/Date code line, Thermal Characteristics, pin description and Ordering Information
0.5	2022-04-29	Yi-Tao.Tsai	Fix Typo at Page-7 and Page-3
0.6	2022-06-14	Yi-Tao.Tsai	Fix Typo at Page-3: block diagram Add power on sequence parameters table
0.7	2022-07-01	Yi-Tao.Tsai	Add I2S to feature list
0.8	2022-07-13	Yi-Tao.Tsai	Fix pin share table for I2S Fix Table 2 2 Pin Description
0.9	2022-09-16	Yi-Tao.Tsai	Fix pin descriptions
0.92	2022-09-28	Yi-Tao.Tsai	Fix pin descriptions (PCIE_PRESET_N)
1.0	2022-11-07	Yi-Tao.Tsai	Modify eMMC4.5 to eMMC4.5/SD in features Update SPI Master AC timing Only support SGMII-1 or Internal GBE due to MAC sharing Add WiFi STA number in features
1.1	2022-11-09	Yi-Tao.Tsai	eMMC @ 52MHz 3.3V
1.2	2023-03-08	Yi-Tao.Tsai	Add DC Characteristics of IO
1.3	2023-03-22	Yi-Tao.Tsai	Remove SPI NOR, it can refer to 3.6.2 SPI interface

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1 General Features

1.1 Platform Features

- **AP MCU subsystem**
  - Dual-core ARM® Cortex-A53 MPCoreTM operating at 1.3 GHz
  - NEON processing engine with Advanced SIMD and Floating-point Extension
  - 32KB L1 I-cache and 32KB L1 D-cache
  - 256KB unified L2 cache
  - Cryptography Extension
- **WIFI MCU subsystem**
  - Andes N13 processor with I/D cache
- **Memory interface**
  - 16-bit data bus width
  - Memory clock up to DDR3/DDR4-2133
  - Supports self-refresh/partial self-refresh mode
  - Programmable slew rate for memory controller's IO pads
  - Advanced bandwidth arbitration control
- **External interface**
  - 1 USB3.0/USB2.0 (Host)
  - UART for external devices and debugging interfaces
  - SPI master for external devices
  - SPI NOR flash interface
  - SPI NAND flash interface
  - eMMC4.5/SD inferface
  - I2C to control peripheral devices
  - General Purpose Input/Output
  - PWM (Pulse Width Modulation)
- **Operating conditions**
  - Core voltage: 0.87V
  - I/O voltage: 1.8V/3.3V
  - DRAM Memory: 1.5V/1.8V
  - Clock source: 40MHz
- **Package**
  - TFBGA 13.0x11.7mm
  - Ball Pitch: 0.65mm

1.2 Wireless Connectivity Features

1.2.1 Wi-Fi MAC

1.2.1.1 Features

Wi-Fi MAC supports the following features:

- Support Dual band Dual Concurrent
- Support all date rates of 802.11a/b/g/n/ac/ax
- Support short GI and all data rates of 802.11n including MCS0 to MCS7
- Support 802.11ac MCS0 to MCS11
- Support 802.11ax MCS0 to MCS11
- AMPDU/AMSDU RX (de-aggregation) and TX (aggregation) support
- TX beamformer and RX beamformee
- TX rate adaptation
- TX power control
- Security
  - 64-bit WEP (WEP-40) and 128-bit WEP (WEP-104) encryption with hardware TKIP processing
  - AES-CCMP hardware processing
  - GCMP hardware processing
- Management/control frame filtering

1.2.2 WLAN Baseband

1.2.2.1 Features

Wi-Fi baseband supports the following features:

- Support Dual band Dual Concurrent
- 20/40/80/160 MHz channels
- HE MCS0-11 BW20/40/80/160MHz with Nss=1~2
- Short Guard Interval
- Space-time block code (STBC)
- Low Density Parity check (LDPC)
- Support digital pre-distortion to enhance PA performance
- Smoothing (channel estimation) extension to MIMO case
- Support radar detection
- Beamformer (explicit/implicit)
  - Eecoded BW20/40/80/160 up to 2x2 BF matrix apply
- Beamformee
  - Decoded BW20/40/80/160 up to 4x2 MU matrix feedback
- UL OFDMA / MU-MIMO
- DL OFDMA / MU-MIMO
- Max RU number in 2G band is 8
- Max RU number in 5G band is 16
- Max User number is 256

1.3 Wired Ethernet Features

- **Frame Engine**
  - Packet DMA (PDMA)
    - 4 Tx descriptor and 4 Rx descriptor rings
    - Scattter/Gather DMA
    - Configurable 4/8/16/32 32-bit burst legnth and delayed interrupt
    - Support TSO
  - QoS DMA (QDMA)
    - Supports 64 Tx physical queues and 4 sets of scheduler
    - Per Tx queue forward/drop packet accounting
    - Per Tx queue forward byte accounting
    - Supports Tx queue min/max rate control and SP/WFQ egress scheduler
    - Supports up to 1024 virtual queues for 8 sets of SFQ
  - Packet Switch Engine (PSE)
    - Wire-speed NAT/NAPT routing
    - Egress rate limiting/shaping
    - IP/TCP/UDP checksum offload
    - IP/TCP/UDP checksum generaton
    - VLAN & PPPoE header insertion
    - TCP segmentation offload
  - Packet Process Engine (PPE)
    - IPv4 NAP/NAPT, IPv6 Routing and Tunnel IP (DS-Lite, 6RD, 464XLAT, MAP-E/T)
    - 1/2/4/8/16/32K session/flow
    - Flow offloading technology for flexible/high performance packet L3/L4 packet processing
    - Support NAT/NAPT wire-speed within 128 flows for any packet size

  Note that PPE features mentioned above require software porting to function.

- **WiFi WARP**
  - Ethernet/WiFi offlaod, forwarding packet directly
  - Dynamic buffer allocate and release

- **GigaMAC (GMAC)**
  - Support IEEE 802.3x full duplex flow control
  - Integrate 1G PHY for extender.
  - Only support SGMII-1 or Internal-GBE due to their MAC sharing.
  - Support HSGMII interface
    - HSGMII supports 10/100/1000Mbps speed change through auto negotiation and configurable 2.5Gbps SerDes link

1.4 Main Features Summary

The following table covers the main features offered by MT7981B.

Table 1-1 Main Features

Feature	Description
CPU	ARM CA53 (1.3GHz, Dual-core)
I-Cache, D-Cache	32kB, 32kB per core
L2 Cache	256KB
Security	Support 2* 256-bit Multi-key on OTP efuse Support 64 versions OTP efuse for Anti-roll back
DRAM data	16bit (external memory interface)
External DDR3/DDR4	2133 Mbps (2GB support)
WIFI	2x2 (2ss) 11ax 2.4GHz + 3x3 (2ss) 11ax 5GHz Integrated PA, LNA and TR-SW 20/40/80/160MHz bandwidth Support up to 1024QAM Support external LNA and PA support (option)
Ethernet	HSGMII x 2; Integrate 1G PHY for extender. Only support SGMII-1 or Internal-GBE due to MAC sharing
HNAT/HQoS	HQoS 64 queues, SFQ 1K queues HNAT (IPv4, IPv6 routing, DS-Lite, 6RD)
USB	USB3.0 x 1
SPIM NAND Flash	Use on-die ECC
SPI Flash (NOR)	Max 50MHz data bit width x1/x2/x4 Support 4-byte address mode compatible with 3-byte address mode
eMMC/SD	eMMC v4.5 @52MHz 3.3V
I2S	Support two-channels I2S x 1 Sample rate 8kHz ~ 192kHz
I2C	I2C x 1 100kHz, Support 7/10-bit addressing
SPI	SPI x 1 Support DMA and FIFO mode
UART	UART-Lite(2-pins) x 1 UART(4-pins) x 2
Package	13.0 mm x 11.7 mm, TFBGA

2 Pin

2.1 Ball Map

Table 2-1 Ball Map (DDR3, DDR4)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	NC_A1	WF_HB0	AVDD15_POR	POR_BG_OUT	WF0_QN		AVSS18_WBG				AVSS18_WBG			AVSS18_WBG			WF4_IP	SPI1_MISO	SPI1_CLK	NC_A20	A
B	WF_HB2	WF_HB3	WF_HB4	POR_RSTB	WF0_QP	AVSS18_WBG	WF0_IP	WF1_QP		WF2_QN	WF2_QP		WF3_QN	WF3_IN	AVSS18_WBG	WF4_QP	WF4_IN	SPI1_MOSI	SPI0_HOLD	SPI0_CS	B
C	WF_TOP_DATA	WF_XO_REQ	WF_HB1	AVDD18_POR	WF_HB5	AVSS18_WBG	WF0_IN	WF1_QN	WF1_IN	WF1_IP	WF2_IN	WF2_IP	WF3_QP	WF3_IP	WF4_QN	AVSS18_WBG	SPI1_CS	SPI0_MISO	SPI0_WP		C
D		WF_CBA_RESETB	WF_DIG_RESETB	GNDK	WF_HB0_B	WF_HB6	WF_HB8	AVSS18_WBG	AVSS18_WBG	AVSS18_WBG	AVSS18_WBG	AVSS18_WBG	AVSS18_WBG	AVSS18_WBG	AVSS18_WBG	MAIN_X40M_IN	GNDK	SPI0_MOSI	SPI0_CLK	PWM0	D
E	GNDK	GNDK	WF_TOP_CLK	GNDK	DVDD18_VQPS	WF_HB7	WF_HB9	WF_HB10	AVSS18_WBG	AVSS18_WBG	AVDD12_WBG	AVDD18_WBG	AVSS18_WBG	AVDD18_CKSQ	AVDD12_CKSQ	GNDK	GNDK	GPIO_RESET	TSAUX_MD	AUXIN2	E
F	SGMII1_LN0_TXN	SGMII1_LN0_TXP	GNDK	AVDD18_SGMII	GNDK	DVDD18IO_LT	DVDD18IO_TL	VCCK	VCCK	VCCK	GNDK	GNDK	VCCK	VCCK	DVDD18IO_RTC1	TESTMODE	GPIO_WPS	GNDK	AUXIN0	AUXIN1	F
G	SGMII1_LN0_RXP	SGMII1_LN0_RXN	GNDK	AVDD09_SGMII	GNDK	VCCK	VCCK	GNDK	GNDK	GNDK	GNDK	GNDK	VCCK	DVDD33IO_RTC1	DVDD18IO_RTC0	UART0_RXD	UART0_TXD	GNDK	TSAUX_REFP	AVDD18_AUXADC	G
H	GNDK			GNDK	GNDK	VCCK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	VCCK	DVDD33IO_RTC0	GNDK	GNDK	GNDK	AVDD18_SGMII		H
J		GNDK	GNDK	AVDD18_USB	AVDD18_PLLGP	VCCK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	VCCK	GNDK	GNDK	AVDD09_SGMII	SGMII_LN0_RXP	SGMII_LN0_RXN	J
K		USB_DP	USB_DM	AVDD33_USB	GNDK	DVDD18IO_LB	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	VCCK	GNDK	GNDK	SMI_MDIO	GNDK	SGMII_LN0_TXP	SGMII_LN0_TXN	K
L	PLLGP_TP	PLLGP_TN	USB_VBUS	JTAG_JTDI	JTAG_JTMS	DVDD18IO_BL	DVDD33IO_BL	VCCK	VCCK	VCCK	DVDD_DDR_TX	DVDD_DDR_RX	GNDK	VCCK	DVDD33IO_RB	DVDD18IO_RB	SMI_MDC	GNDK	GNDK	GNDK	L
M	WF2G_LED	WF5G_LED	JTAG_JTDO	JTAG_JTRST_N	GNDK	DVDD33IO_LB	VCCK				VDDIO_DDR_A	VDDIO_DDR_CA	GNDK	VCCK	VCCK	GNDK	GBE_INT	GBE_RESET	GBE_TXVN_D_P0	GBE_TXVP_D_P0	M
N		SYSRSTB		JTAG_JTCLK	GNDK	GNDK	GNDK	VDDIO_DDR_DQ	VDDIO_DDR_DQ	VDDIO_DDR_MCLK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GBE_TXVP_C_P0	GBE_TXVN_C_P0	N
P		WO_JTAG_JTMS	WO_JTAG_JTCLK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	AVDD33_LD_P0	GBE_TXVN_B_P0		P
R	SYS_WATCHDOG	WO_JTAG_JTRST_N	WO_JTAG_JTDO	WO_JTAG_JTDI	GNDK	EMI0_DQ11	EMI0_DQ15	EMI0_DQS1_T	EMI0_DQ14	EMI0_DQ10	EMI0_BA1		EMI0_A10	EMI0_CAS_N	EMI_RESET_N	EMI0_BA2	AVDD18_RDDR	AVDD18_COM	GBE_TXVP_B_P0	GBE_TXVN_A_P0	R
T	SPI2_MISO	SPI2_CLK	SPI2_MOSI	GNDK	EMI0_DM1	EMI0_DQ13	EMI0_DQ9	EMI0_DQS1_C	EMI0_DQ8	EMI0_DQ12	EMI0_A4	EMI0_A8	EMI0_A11	EMI0_A0	EMI0_A9	EMI0_A3	GNDK	GNDK	REXT	GBE_TXVP_A_P0	T
U	SPI2_WP	SPI2_HOLD	GNDK	EMI0_DQ6	EMI0_DQ0	EMI0_DQS0_T	EMI0_DM0	EMI0_DQ3	EMI0_DQ7	EMI0_CK_T	EMI0_CKE0	EMI0_A1	EMI0_A14	EMI0_RAS_N	EMI0_ODT	EMI0_A13	EMI0_A5	EMI0_WE_N	EMI_EXTR	GNDK	U
V	NC_V1	SPI2_CS	GNDK	EMI0_DQ4	EMI0_DQ2	GNDK	EMI0_DQS0_C	EMI0_DQ1	GNDK	EMI0_DQ5	EMI0_CK_C	GNDK	EMI0_A6	EMI0_A12	GNDK	EMI0_A2	EMI0_A7	EMI0_BA0	EMI0_CS0_N	NC_V20	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
P						GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK	GNDK				P
R					GNDK	EMI0_DQ14	EMI0_DQ8	EMI0_DQS1_T	EMI0_DQ11	EMI0_DQ13	EMI0_BA1		EMI0_A12	EMI0_A4	EMI_RESET_N	EMI0_A10	AVDD18_RDDR				R
T				GNDK	EMI0_DM1	EMI0_DQ12	EMI0_DQ10	EMI0_DQS1_C	EMI0_DQ15	EMI0_DQ9	EMI0_A5	EMI0_A13	EMI0_A9	EMI0_A0	EMI0_A11	EMI0_A8	GNDK	GNDK			T
U			GNDK	EMI0_DQ4	EMI0_DQ0	EMI0_DQS0_T	EMI0_DM0	EMI0_DQ3	EMI0_DQ5	EMI0_CK_T	EMI0_CKE0	EMI0_A1	EMI0_A3	EMI0_RAS_N	EMI0_ODT	EMI0_A2	EMI0_BA0	EMI0_WE_N	EMI_EXTR	GNDK	U
V	NC_V1		GNDK	EMI0_DQ6	EMI0_DQ2	GNDK	EMI0_DQS0_C	EMI0_DQ1	GNDK	EMI0_DQ7	EMI0_CK_C	GNDK	EMI0_A7	EMI0_CAS_N	GNDK	EMI0_BG0	EMI0_A6	EMI0_ACT_N	EMI0_CS0_N	NC_V20	V
DDR4	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

2.2 Pin Descriptions

Table 2-2 Pin Description

Pin	Name	Reset *1		After Reset *1				Pull *3, *4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
GPIO											
F17	GPIO_WPS	I	PD	I	0	PD	2	PU/PD	3.3	2/4/8/12/16	General Purpose IO / GPIO_WPS
E18	GPIO_RESET	I	PD	I	0	PD	2	PU/PD	3.3	2/4/8/12/16	General Purpose IO / GPIO_RESET
L3	USB_VBUS	O	H-Z	I	1	PD	4	PU/PD	3.3	2/4/8/12/16	General Purpose IO / USB_DRV_VBUS
N3	PCIE_PERESET_N	O	H-Z	I	1	PD	4	PU/PD	3.3	2/4/8/12/16	General Purpose IO/PCIE_PERESET_N
M4	JTAG_JTRST_N	I	PU	I	1	NP	2	PU/PD	3.3	2/4/8/12/16	General Purpose IO / JTAG_JTRST_N
L4	JTAG_JTDI	I	PU	I	1	NP	2	PU/PD	3.3	2/4/8/12/16	General Purpose IO / JTAG_JTDI
L5	JTAG_JTMS	I	PU	I	1	NP	2	PU/PD	3.3	2/4/8/12/16	General Purpose IO / JTAG_JTMS
N4	JTAG_JTCLK	I	PU	I	1	NP	2	PU/PD	3.3	2/4/8/12/16	General Purpose IO / JTAG_JTCLK
M3	JTAG_JTDO	O	H-Z	I	1	NP	2	PU/PD	3.3	2/4/8/12/16	General Purpose IO / JTAG_JTDO
R3	WO_JTAG_JTDO	I	PD	I	0	NP	2	PU/PD	3.3	2/4/8/12/16	General Purpose IO / WO_JTAG_JTDO
P3	WO_JTAG_JTCLK	I	PD	I	0	NP	2	PU/PD	3.3	2/4/8/12/16	General Purpose IO / WO_JTAG_JTCLK
P2	WO_JTAG_JTMS	I	PD	I	0	NP	2	PU/PD	3.3	2/4/8/12/16	General Purpose IO / WO_JTAG_JTMS
R4	WO_JTAG_JTDI	I	PD	I	0	NP	2	PU/PD	3.3	2/4/8/12/16	General Purpose IO / WO_JTAG_JTDI
R2	WO_JTAG_ JTRST_N	I	PD	I	0	NP	2	PU/PD	3.3	2/4/8/12/16	General Purpose IO / WO_ JTAG_ JTRST_N
UART											
G16	UART0_RXD	I	PU	I	1	PU	2	PU/PD	3.3	2/4/8/12/16	UART RX data
G17	UART0_TXD	O	H-Z	OH	1	PU	2	PU/PD	3.3	2/4/8/12/16	UART TX data
Pulse-Width Modulation(PWM)											
D20	PWM0	O	H-Z	I	0	PD	4	PU/PD	3.3	2/4/8/12/16	PWM0
Serial Flash											
D19	SPI0_CLK	O	H-Z	OL	1	PD	2	PU/PD	3.3	2/4/8/12/16	Serial Flash Clock
B20	SPI0_CS	O	H-Z	OH	1	PU	2	PU/PD	3.3	2/4/8/12/16	Serial Flash Chip Select
D18	SPI0_MOSI	O	H-Z	OL	1	PD	2	PU/PD	3.3	2/4/8/12/16	Serial Flash Master Output, Slave Input
C18	SPI0_MISO	I	PD	I	1	PD	2	PU/PD	3.3	2/4/8/12/16	Serial Flash Master Input, Slave Output
C19	SPI0_WP	I	PU	I	1	PD	2	PU/PD	3.3	2/4/8/12/16	Serial Flash Write Protect
B19	SPI0_HOLD	I	PU	I	1	PU	2	PU/PD	3.3	2/4/8/12/16	Serial Flash HOLD
A19	SPI1_CLK	I	PD	OL	1	PD	2	PU/PD	3.3	2/4/8/12/16	Serial Flash Clock
C17	SPI1_CS	I	PU	OH	1	PU	2	PU/PD	3.3	2/4/8/12/16	Serial Flash Chip Select
B18	SPI1_MOSI	O	H-Z	I	1	PD	2	PU/PD	3.3	2/4/8/12/16	Serial Flash Master Output, Slave Input
A18	SPI1_MISO	I	PD	I	1	PD	2	PU/PD	3.3	2/4/8/12/16	Serial Flash Master Input, Slave Output
T2	SPI2_CLK	O	H-Z	OL	1	PD	2	PU/PD	3.3	2/4/8/12/16	Serial Flash Clock
V2	SPI2_CS	O	H-Z	OH	1	PU	2	PU/PD	3.3	2/4/8/12/16	Serial Flash Chip Select
T3	SPI2_MOSI	O	H-Z	OL	1	PD	2	PU/PD	3.3	2/4/8/12/16	Serial Flash Master Output, Slave Input
T1	SPI2_MISO	I	PD	I	1	PD	2	PU/PD	3.3	2/4/8/12/16	Serial Flash Master Input, Slave Output
U1	SPI2_WP	I	PU	I	1	PD	2	PU/PD	3.3	2/4/8/12/16	Serial Flash Write Protect
U2	SPI2_HOLD	I	PU	I	1	PU	2	PU/PD	3.3	2/4/8/12/16	Serial Flash HOLD

Pin	Name	Reset *1		After Reset *1				Pull *3, *4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
DRAM											
U19	EMI_EXTR	A	-	A	-	-	-	-	1.5	-	DRAM calibration resistor
R15	EMI_RESET_N	A	-	A	-	-	-	-	1.5	-	DRAM Signal
T14	EMI0_A0	A	-	A	-	-	-	-	1.5	-	DRAM Signal
U12	EMI0_A1	A	-	A	-	-	-	-	1.5	-	DRAM Signal
R13	EMI0_A10	A	-	A	-	-	-	-	1.5	-	DRAM Signal
T13	EMI0_A11	A	-	A	-	-	-	-	1.5	-	DRAM Signal
V14	EMI0_A12	A	-	A	-	-	-	-	1.5	-	DRAM Signal
U16	EMI0_A13	A	-	A	-	-	-	-	1.5	-	DRAM Signal
U13	EMI0_A14	A	-	A	-	-	-	-	1.5	-	DRAM Signal
V16	EMI0_A2	A	-	A	-	-	-	-	1.5	-	DRAM Signal
T16	EMI0_A3	A	-	A	-	-	-	-	1.5	-	DRAM Signal
T11	EMI0_A4	A	-	A	-	-	-	-	1.5	-	DRAM Signal
U17	EMI0_A5	A	-	A	-	-	-	-	1.5	-	DRAM Signal
V13	EMI0_A6	A	-	A	-	-	-	-	1.5	-	DRAM Signal
V17	EMI0_A7	A	-	A	-	-	-	-	1.5	-	DRAM Signal
T12	EMI0_A8	A	-	A	-	-	-	-	1.5	-	DRAM Signal
T15	EMI0_A9	A	-	A	-	-	-	-	1.5	-	DRAM Signal
V18	EMI0_BA0	A	-	A	-	-	-	-	1.5	-	DRAM Signal
R11	EMI0_BA1	A	-	A	-	-	-	-	1.5	-	DRAM Signal
R16	EMI0_BA2	A	-	A	-	-	-	-	1.5	-	DRAM Signal
R14	EMI0_CAS_N	A	-	A	-	-	-	-	1.5	-	DRAM Signal
V11	EMI0_CK_C	A	-	A	-	-	-	-	1.5	-	DRAM Signal
U10	EMI0_CK_T	A	-	A	-	-	-	-	1.5	-	DRAM Signal
U11	EMI0_CKE0	A	-	A	-	-	-	-	1.5	-	DRAM Signal
V19	EMI0_CS0_N	A	-	A	-	-	-	-	1.5	-	DRAM Signal
U7	EMI0_DM0	A	-	A	-	-	-	-	1.5	-	DRAM Signal
T5	EMI0_DM1	A	-	A	-	-	-	-	1.5	-	DRAM Signal
U5	EMI0_DQ0	A	-	A	-	-	-	-	1.5	-	DRAM Signal
V8	EMI0_DQ1	A	-	A	-	-	-	-	1.5	-	DRAM Signal
R10	EMI0_DQ10	A	-	A	-	-	-	-	1.5	-	DRAM Signal
R6	EMI0_DQ11	A	-	A	-	-	-	-	1.5	-	DRAM Signal
T10	EMI0_DQ12	A	-	A	-	-	-	-	1.5	-	DRAM Signal
T6	EMI0_DQ13	A	-	A	-	-	-	-	1.5	-	DRAM Signal
R9	EMI0_DQ14	A	-	A	-	-	-	-	1.5	-	DRAM Signal
R7	EMI0_DQ15	A	-	A	-	-	-	-	1.5	-	DRAM Signal
V5	EMI0_DQ2	A	-	A	-	-	-	-	1.5	-	DRAM Signal
U8	EMI0_DQ3	A	-	A	-	-	-	-	1.5	-	DRAM Signal
V4	EMI0_DQ4	A	-	A	-	-	-	-	1.5	-	DRAM Signal
V10	EMI0_DQ5	A	-	A	-	-	-	-	1.5	-	DRAM Signal
U4	EMI0_DQ6	A	-	A	-	-	-	-	1.5	-	DRAM Signal

Pin	Name	Reset *1		After Reset *1				Pull *3, *4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
U9	EMI0_DQ7	A	-	A	-	-	-	-	1.5	-	DRAM Signal
T9	EMI0_DQ8	A	-	A	-	-	-	-	1.5	-	DRAM Signal
T7	EMI0_DQ9	A	-	A	-	-	-	-	1.5	-	DRAM Signal
V7	EMI0_DQS0_C	A	-	A	-	-	-	-	1.5	-	DRAM Signal
U6	EMI0_DQS0_T	A	-	A	-	-	-	-	1.5	-	DRAM Signal
T8	EMI0_DQS1_C	A	-	A	-	-	-	-	1.5	-	DRAM Signal
R8	EMI0_DQS1_T	A	-	A	-	-	-	-	1.5	-	DRAM Signal
U15	EMI0_ODT	A	-	A	-	-	-	-	1.5	-	DRAM Signal
U14	EMI0_RAS_N	A	-	A	-	-	-	-	1.5	-	DRAM Signal
U18	EMI0_WE_N	A	-	A	-	-	-	-	1.5	-	DRAM Signal
(SSUSB or SGMII1) / USB											
G1	SGMII1_LN0_RXP	A	-	A	-	-	-	-	0.9	-	SSUSB/SGMII1 data pin RX +
G2	SGMII1_LN0_RXN	A	-	A	-	-	-	-	0.9	-	SSUSB/SGMII1 data pin RX -
F2	SGMII1_LN0_TXP	A	-	A	-	-	-	-	0.9	-	SSUSB/SGMII1 data pin TX +
F1	SGMII1_LN0_TXN	A	-	A	-	-	-	-	0.9	-	SSUSB/SGMII1 data pin TX -
K3	USB_DM	A	-	A	-	-	-	-	3.3	-	USB HS/FS/LS data pin Data -
K2	USB_DP	A	-	A	-	-	-	-	3.3	-	USB HS/FS/LS data pin Data +
Serial Management Interface (SMI)											
L17	SMI_MDC	O	H-Z	OL	1	PU	2	PU/PD	3.3	2/4/8/12/16	Serial management clock
K17	SMI_MDIO	I	PU	I	1	PU	2	PU/PD	3.3	2/4/8/12/16	Serial management data
GBE Interface											
M18	GBE_RESET	I	PD	I	0	PD	2	PU/PD	3.3	2/4/8/12/16	GBE_RESET
M17	GBE_INT	I	PD	I	1	PD	2	PU/PD	3.3	2/4/8/12/16	GBE_INT
Thermal Sensor Interface (TSAUX)											
F19	AUXIN0	A	-	A	-	-	-	-	1.8	-	Aux ADC input 0
F20	AUXIN1	A	-	A	-	-	-	-	1.8	-	Aux ADC input 1
E20	AUXIN2	A	-	A	-	-	-	-	1.8	-	Aux ADC input 2
E19	TSAUX_MD	A	-	A	-	-	-	-	1.8	-	TSAUX_MD
G19	TSAUX_REFP	A	-	A	-	-	-	-	1.8	-	TSAUX_REFP
SGMII											
J20	SGMII_LN0_RXN	A	-	A	-	-	-	-	0.9	-	SGMII 0 data pin RX -
J19	SGMII_LN0_RXP	A	-	A	-	-	-	-	0.9	-	SGMII 0 data pin RX +
K20	SGMII_LN0_TXN	A	-	A	-	-	-	-	0.9	-	SGMII 0 data pin TX -
K19	SGMII_LN0_TXP	A	-	A	-	-	-	-	0.9	-	SGMII 0 data pin TX +
GPHY/GBE interface											
T19	REXT	A	-	A	-	-	-	-	1.8	-	REXT
T20	GBE_TXVP_A_P0	A	-	A	-	-	-	-	3.3	-	GPHY A_Channel differential P node
R20	GBE_TXVN_A_P0	A	-	A	-	-	-	-	3.3	-	GPHY A_Channel differential N node
R19	GBE_TXVP_B_P0	A	-	A	-	-	-	-	3.3	-	GPHY B_Channel differential P node
P19	GBE_TXVN_B_P0	A	-	A	-	-	-	-	3.3	-	GPHY B_Channel differential N node
N19	GBE_TXVP_C_P0	A	-	A	-	-	-	-	3.3	-	GPHY C_Channel differential P node

Pin	Name	Reset *1		After Reset *1				Pull *3, *4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
N20	GBE_TXVN_C_P0	A	-	A	-	-	-	-	3.3	-	GPHY C_Channel differential N node
M20	GBE_TXVP_D_P0	A	-	A	-	-	-	-	3.3	-	GPHY D_Channel differential P node
M19	GBE_TXVN_D_P0	A	-	A	-	-	-	-	3.3	-	GPHY D_Channel differential N node
OSC Clock											
D16	MAIN_X40M_XIN	A	-	A	-	-	-	-	1.8	-	OSC clock input
WiFi IF (2.4G/5G)											
E3	WF_TOP_CLK	I	PD	OH	1	NP	4	PU/PD	1.8	2/4/8/12/16	SPI clock
C1	WF_TOP_DATA	I	PD	OH	1	NP	4	PU/PD	1.8	2/4/8/12/16	SPI data
A2	WF_HB0	I	PD	OL	1	NP	4	PU/PD	1.8	2/4/8/12/16	WRI clock
D5	WF_HB0_B	I	PD	OL	1	NP	4	PU/PD	1.8	2/4/8/12/16	WRI clock
C3	WF_HB1	I	PD	OL	1	NP	4	PU/PD	1.8	2/4/8/12/16	WRI wf0 data[0]
B1	WF_HB2	I	PD	OL	1	NP	4	PU/PD	1.8	2/4/8/12/16	WRI wf0 data[1]
B2	WF_HB3	I	PD	OL	1	NP	4	PU/PD	1.8	2/4/8/12/16	WRI wf1 data[0]
B3	WF_HB4	I	PD	OL	1	NP	4	PU/PD	1.8	2/4/8/12/16	WRI wf1 data[1]
C5	WF_HB5	I	PD	OL	1	NP	4	PU/PD	1.8	2/4/8/12/16	WRI wf2 data[0]
D6	WF_HB6	I	PD	OL	1	NP	4	PU/PD	1.8	2/4/8/12/16	WRI wf2 data[1]
E6	WF_HB7	I	PD	OL	1	NP	4	PU/PD	1.8	2/4/8/12/16	WRI wf3 data[0]
D7	WF_HB8	I	PD	OL	1	NP	4	PU/PD	1.8	2/4/8/12/16	WRI wf3 data[1]
E7	WF_HB9	I	PD	OL	1	NP	4	PU/PD	1.8	2/4/8/12/16	WRI wf4 data[0]
E8	WF_HB10	I	PD	OL	1	NP	4	PU/PD	1.8	2/4/8/12/16	WRI wf4 data[1]
C2	WF_XO_REQ	I	PD	OH	1	NP	4	PU/PD	1.8	2/4/8/12/16	OSC clock request to RF chip
D3	WF_DIG_RESETB	I	PD	OH	1	NP	4	PU/PD	1.8	2/4/8/12/16	Reset RF chip digital
D2	WF_CBA_RESETB	I	PD	OH	1	NP	4	PU/PD	1.8	2/4/8/12/16	Reset RF chip analog
M1	WF2G_LED	O	H-Z	I	0	PD	2	PU/PD	3.3	2/4/8/12/16	2G LED
M2	WF5G_LED	O	H-Z	I	0	PD	2	PU/PD	3.3	2/4/8/12/16	5G LED
A17	WF4_IP	A	-	A	-	-	-	-	1.8	-	WF4 I_Channel differential P node
B17	WF4_IN	A	-	A	-	-	-	-	1.8	-	WF4 I_Channel differential N node
B16	WF4_QP	A	-	A	-	-	-	-	1.8	-	WF4 Q_Channel differential P node
C15	WF4_QN	A	-	A	-	-	-	-	1.8	-	WF4 Q_Channel differential N node
C14	WF3_IP	A	-	A	-	-	-	-	1.8	-	WF3 I_Channel differential P node
B14	WF3_IN	A	-	A	-	-	-	-	1.8	-	WF3 I_Channel differential N node
C13	WF3_QP	A	-	A	-	-	-	-	1.8	-	WF3 Q_Channel differential P node
B13	WF3_QN	A	-	A	-	-	-	-	1.8	-	WF3 Q_Channel differential N node
C12	WF2_IP	A	-	A	-	-	-	-	1.8	-	WF2 I_Channel differential P node
C11	WF2_IN	A	-	A	-	-	-	-	1.8	-	WF2 I_Channel differential N node
B11	WF2_QP	A	-	A	-	-	-	-	1.8	-	WF2 Q_Channel differential P node
B10	WF2_QN	A	-	A	-	-	-	-	1.8	-	WF2 Q_Channel differential N node
C10	WF1_IP	A	-	A	-	-	-	-	1.8	-	WF1 I_Channel differential P node
C9	WF1_IN	A	-	A	-	-	-	-	1.8	-	WF1 I_Channel differential N node
B8	WF1_QP	A	-	A	-	-	-	-	1.8	-	WF1 Q_Channel differential P node
C8	WF1_QN	A	-	A	-	-	-	-	1.8	-	WF1 Q_Channel differential N node

Pin	Name	Reset *1		After Reset *1				Pull *3, *4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
B7	WF0_IP	A	-	A	-	-	-	-	1.8	-	WF0 I_Channel differential P node
C7	WF0_IN	A	-	A	-	-	-	-	1.8	-	WF0 I_Channel differential N node
B5	WF0_QP	A	-	A	-	-	-	-	1.8	-	WF0 Q_Channel differential P node
A5	WF0_QN	A	-	A	-	-	-	-	1.8	-	WF0 Q_Channel differential N node
POR											
B4	POR_RSTB	A	-	A	-	-	-	-	1.8	-	PMU_RSTB
A4	POR_BG_OUT	A	-	A	-	-	-	-	1.8	-	BG_OUT
PLLGP											
L1	PLLGP_TP	A	-	A	-	-	-	-	1.8	-	PLLGP_TP test point
L2	PLLGP_TN	A	-	A	-	-	-	-	1.8	-	PLLGP_TN test point
MISC											
R1	SYS_WATCHDOG	OL	-	OH	-	-	-	-	3.3	-	Watchdog reset
N2	SYSRSTB	I	PU	I	-	PU	-	PU	3.3	-	Power on reset
F16	TESTMODE	I	PD	I	-	PD	-	PD	3.3	-	Test mode
POWER											
F8, F9, F10,F13, F14,G6, G7, G13, H6, H14, J6,J15, K14, L8, L9, L10, L14, M7, M14, M15	VCCK	P	-	P	-	-	-	-	0.85	-	Core power supply (DVDD_CORE)
F7 F6 K6 L6 L16 G15 F15	DVDD18IO_TL DVDD18IO_LT DVDD18IO_LB DVDD18IO_BL DVDD18IO_RB DVDD18IO_RTC0 DVDD18IO_RTC1	P	-	P	-	-	-	-	1.8	-	IO power supply
M6 L7 L15 H15 G14	DVDD33IO_LB DVDD33IO_BL DVDD33IO_RB DVDD33IO_RTC0 DVDD33IO_RTC1	P	-	P	-	-	-	-	3.3	-	IO power supply
G4	AVDD09_SGMII	P	-	P	-	-	-	-	0.9	-	SGMII1 power supply
J18	AVDD09_SGMII	P	-	P	-	-	-	-	0.9	-	SGMII power supply
F4	AVDD18_SGMII	P	-	P	-	-	-	-	1.8	-	SGMII1 power supply
H19	AVDD18_SGMII	P	-	P	-	-	-	-	1.8	-	SGMII power supply
A3	AVDD15_POR	P	-	P	-	-	-	-	1.5	-	POR power supply
C4	AVDD18_POR	P	-	P	-	-	-	-	1.8	-	POR power supply
E15	AVDD12_CKSQ	P	-	P	-	-	-	-	1.2	-	CKSQ power supply
E14	AVDD18_CKSQ	P	-	P	-	-	-	-	1.8	-	CKSQ power supply
G20	AVDD18_AUXADC	P	-	P	-	-	-	-	1.8	-	TSAUX power supply
J5	AVDD18_PLLGP	P	-	P	-	-	-	-	1.8	-	PLLGP power supply

Pin	Name	Reset *1		After Reset *1				Pull *3, *4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
R17	AVDD18_RDDR	P	-	P	-	-	-	-	1.8	-	DDR power supply
M11	VDDIO_DDR_R	P	-	P	-	-	-	-	1.5	-	DDR power supply
M12	VDDIO_DDR_CA	P	-	P	-	-	-	-	1.5	-	DDR power supply
N8	VDDIO_DDR_DQ	P	-	P	-	-	-	-	1.5	-	DDR power supply
N9	VDDIO_DDR_DQ	P	-	P	-	-	-	-	1.5	-	DDR power supply
N10	VDDIO_DDR_MCLK	P	-	P	-	-	-	-	1.5	-	DDR power supply
L11	DVDD_DDR_TX	P	-	P	-	-	-	-	0.87		DDR core power supply
L12	DVDD_DDR_RX	P	-	P	-	-	-	-	0.87		DDR core power supply
J4	AVDD18_USB	P	-	P	-	-	-	-	1.8	-	USB power supply
K4	AVDD33_USB	P	-	P	-	-	-	-	3.3	-	USB power supply
E11	AVDD12_WBG	P	-	P	-	-	-	-	1.2	-	AFE power supply
E12	AVDD18_WBG	P	-	P	-	-	-	-	1.8	-	AFE power supply
R18	AVDD18_COM	P	-	P	-	-	-	-	1.8	-	GPHY power supply
P18	AVDD33_LD_P0	P	-	P	-	-	-	-	3.3	-	GPHY power supply
E5	DVDD18_VQPS	P	-	P	-	-	-	-	1.8	-	EFUSE Blow power supply
GROUND											
D4, D17, E1,E2, E4,E16, E17,F3, F5,F11, F12,F18, G3, G5 G8, G9 G10, G11 G12, G18 H1,H4, H5, H7, H8, H9, H10, H11, H12, H13, H16, H17, H18, J2, J3, J7, J8, J9, J10, J11, J12,J13, J14,J16, J17, K5, K7, K8, K9, K10, K11, K12, K13, K15, K16, K18, L13, L18, L19, L20, M5,M13, M16,N5, N6, N7, N11, N12, N13,N14, N15, N16, N17, N18, P4, P5, P6, P7, P8,P9, P10,P11, P12,P13,	GNDK	G	-	G	-	-	-	-	-	-	Ground (DVSS)

Pin	Name	Reset *1		After Reset *1				Pull *3, *4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
P14,P15, P16,P17, R5,T4, T17,T18, U3, U20, V3,V6, V9,V12, V15											
A7, A11, A14, B6, B15, C6, C16, D8, D9, D10, D11,D12, D13,D14, D15,E9, E10, E13	AVSS18_WBG	G	-	G	-	-	-	-	-	-	Ground
A1 A20 V1 V20	NC_A1 NC_A20 NC_V1 NC_V20	-	-	-	-	-	-	-	-	-	NC ball

NOTE:

1. I: Input
   OH: Output high
   OL: Output low
   A: Analog
   P: Power
   G: Ground
   NC: No connection
2. The internal pull resistance range is from 10 kΩ to 75KΩ depend on IO configuration.
3. PD: Internal pull-down
   PU: Internal pull-up
   NP: No pull-down/up
4. While IO is set as GPIO mode, the IO driving strength can be one of 2/4/6/8/10/12/14/16 mA and default is [ ] mA.

2.2.1 Constant Tie Pins

Table 2-3 Constant tied pins

Pin name	Description
TESTMODE	Test mode (tie to GND)

2.3 Pin Sharing Schemes

Some pins are shared with GPIO to provide maximum flexibility for system designers. User can configure register to specify the pin function.

2.3.1 Pin share scheme

Table 2-4 Pin Share

Pin Name	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4
GPIO_WPS	B:GPIO0		I0:WA_AICE_TCKC	I0:WM_AICE_TCKC	
GPIO_RESET	B:GPIO1		B0:WA_AICE_TMSC	B0:WM_AICE_TMSC	
SYS_WATCHDOG	B:GPIO2	O:SYS_WATCHDOG			
JTAG_JTDO	B:GPIO4	O:JTAG_JTDO	O:WM_JTAG_JTDO	I1:UART2_RXD	I0:PTA_EXT_ACT
JTAG_JTDI	B:GPIO5	I1:JTAG_JTDI	I1:WM_JTAG_JTDI	O:UART2_TXD	I0:PTA_EXT_PRI
JTAG_JTMS	B:GPIO6	B1:JTAG_JTMS	I1:WM_JTAG_JTMS	I1:UART2_CTS	O:PTA_EXT_WLAN_ACT
JTAG_JTCLK	B:GPIO7	I1:JTAG_JTCLK	I1:WM_JTAG_JTCLK	O:UART2_RTS	O:PWM2
JTAG_JTRST_N	B:GPIO8	I0:JTAG_JTRST_N	I0:WM_JTAG_JTRST_N	O:GBE_LED0	O:NET_WO0_UART_TXD
WO_JTAG_JTDO	B:GPIO9	O:WO0_JTAG_JTDO	I0:WM_AICE_TCKC		O:PCM_DTX (Note1)
WO_JTAG_JTDI	B:GPIO10	I1:WO0_JTAG_JTDI	B0:WM_AICE_TMSC		I0:PCM_DRX (Note1)
WO_JTAG_JTMS	B:GPIO11	B1:WO0_JTAG_JTMS			O:PCM_CLK (Note1)
WO_JTAG_JTCLK	B:GPIO12	I1:WO0_JTAG_JTCLK			O:PCM_FS (Note1)
WO_JTAG_JTRST_N	B:GPIO13	I0:WO0_JTAG_JTRST_N	O:PWM0	O:GBE_LED1	O:PCM_MCK (Note1)
USB_VBUS	B:GPIO14	O:DRV_VBUS	O:PWM1	O:NET_WO0_UART_TXD	
PWM0	B:GPIO15	O:PWM0	O:EMMC_RSTB	O:PWM1	O:NET_WO0_UART_TXD
SPI0_CLK	B:GPIO16	O:SPI0_CLK	B1:EMMC_DAT0	O:SNFI_CLK	I1:UART1_RXD
SPI0_MOSI	B:GPIO17	B0:SPI0_MOSI	B1:EMMC_DAT1	B0:SNFI_MOSI	O:UART1_TXD
SPI0_MISO	B:GPIO18	B0:SPI0_MISO	B1:EMMC_DAT2	B0:SNFI_MISO	I1:UART1_CTS
SPI0_CS	B:GPIO19	O:SPI0_CS	B1:EMMC_DAT3	O:SNFI_CS	O:UART1_RTS
SPI0_HOLD	B:GPIO20	B0:SPI0_HOLD	B1:EMMC_DAT4	B0:SNFI_HOLD	O:WM_UART_TXD
SPI0_WP	B:GPIO21	B0:SPI0_WP	B1:EMMC_DAT5	B0:SNFI_WP	O:WA_UART_TXD
SPI1_CLK	B:GPIO22	O:SPI1_CLK	B1:EMMC_DAT6	I1:UART2_RXD	I0:PTA_EXT_ACT
SPI1_MOSI	B:GPIO23	O:SPI1_MOSI	B1:EMMC_DAT7	O:UART2_TXD	I0:PTA_EXT_PRI
SPI1_MISO	B:GPIO24	I0:SPI1_MISO	B1:EMMC_CMD	I1:UART2_CTS	O:PTA_EXT_WLAN_ACT
SPI1_CS	B:GPIO25	O:SPI1_CS	B1:EMMC_CLK	O:UART2_RTS	O:PCM_MCK (Note1)
SPI2_CLK	B:GPIO26	O:SPI2_CLK	I1:UART1_RXD		
SPI2_MOSI	B:GPIO27	B0:SPI2_MOSI	O:UART1_TXD		
SPI2_MISO	B:GPIO28	B0:SPI2_MISO	I1:UART1_CTS	I0:WA_AICE_TCKC	
SPI2_CS	B:GPIO29	O:SPI2_CS	O:UART1_RTS	B0:WA_AICE_TMSC	
SPI2_HOLD	B:GPIO30	B0:SPI2_HOLD	O:WF2G_LED	O:WM_UART_TXD	B1:I2C_SCL
SPI2_WP	B:GPIO31	B0:SPI2_WP	O:WF5G_LED	O:WA_UART_TXD	B1:I2C_SDA
UART0_RXD	B:GPIO32	I1:UART0_RXD	B1:SGMII1_PHY_I2C_SCL	B1:U3_PHY_I2C_SCL	
UART0_TXD	B:GPIO33	O:UART0_TXD	B1:SGMII1_PHY_I2C_SDA	B1:U3_PHY_I2C_SDA	
WF2G_LED	B:GPIO34	O:WF2G_LED	B1:XXX_CLK_REQ		
WF5G_LED	B:GPIO35	O:WF5G_LED	I1:XXX_WAKE_N		
SMI_MDC	B:GPIO36	O:SMI_MDC	B1:I2C_SCL	I1:GBE_EXT_MDC	
SMI_MDIO	B:GPIO37	B0:SMI_MDIO	B1:I2C_SDA	B1:GBE_EXT_MDIO	

Pin Name	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4
GBE_INT	B:GPIO38	I0:MT7531_INT			
GBE_RESET	B:GPIO39				
WF_DIG_RESETB	B:GPIO40	O:WF0_DIG_RESETB			
WF_CBA_RESETB	B:GPIO41	O:WF0_CBA_RESETB			
WF_XO_REQ	B:GPIO42	O:WF0_XO_REQ			
WF_TOP_CLK	B:GPIO43	O:WF0_TOP_CLK			
WF_TOP_DATA	B:GPIO44	B0:WF0_TOP_DATA			
WF_HB1	B:GPIO45	B0:WF_HB1	O:WF0_MODE_SEL_1		
WF_HB2	B:GPIO46	B0:WF_HB2	O:WF0_MODE_SEL_2		
WF_HB3	B:GPIO47	B0:WF_HB3	O:WF0_XTAL_SEL_0		
WF_HB4	B:GPIO48	B0:WF_HB4	O:WF0_XTAL_SEL_1		
WF_HB0	B:GPIO49	O:WF_O_HB0	O:WF0_MODE_SEL_0		
WF_HB0_B	B:GPIO50	O:WF_O_HB0_B			
WF_HB5	B:GPIO51	B0:WF_HB5	O:WF0_XTAL_SEL_2		
WF_HB6	B:GPIO52	B0:WF_HB6			
WF_HB7	B:GPIO53	B0:WF_HB7			
WF_HB8	B:GPIO54	B0:WF_HB8			
WF_HB9	B:GPIO55	B0:WF_HB9			
WF_HB10	B:GPIO56	B0:WF_HB10			

Note1: pin share

PCM_DTX: I2S Data Out
PCM_DRX: I2S Data In
PCM_CLK: I2S BCLK/SCK
PCM_FS: I2S WS/LRCK
PCM_MCK: I2S MCLK

2.4 Strapping Options

Table 2-5 Strapping

Pin Name	Strapping Name	Description
USB_VBUS	Boot Mode	{PWM0, USB_VBUS} 00 : SPI-NOR 01 : SPI-NAND → SD 10 : EMMC 11 : SNAND(SNFI) → SD
PWM0		
SPI2_CLK	A-die Crystal	0 : 80MHz 1 : 40MHz

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Symbol or Pin name	Description	Min.	Max.	Unit
VCCK (DVDD_CORE) DVDD_DDR_TX DVDD_DDR_RX	0.87V supply voltage	-0.3	0.95	V
DVDD18IO_TL DVDD18IO_LT DVDD18IO_LB DVDD18IO_BL DVDD18IO_RB DVDD18IO_RTC0 DVDD18IO_RTC1	1.8V supply voltage	-0.3	1.98	V
DVDD33IO_LB DVDD33IO_BL DVDD33IO_RB DVDD33IO_RTC0 DVDD33IO_RTC1	3.3V supply voltage	-0.3	3.6	V
AVDD33_USB AVDD33_LD_P0	3.3V supply voltage	-0.3	3.6	V
AVDD12_CKSQ AVDD12_WBG	1.2V supply voltage	-0.3	1.32	V
AVDD09_SGMII AVDD09_SGMII	0.9V supply voltage	-0.3	0.99	V
AVDD18_SGMII AVDD18_SGMII AVDD18_COM AVDD18_POR AVDD18_AUXADC AVDD18_PLLGP AVDD18_CKSQ AVDD18_USB AVDD18_WBG AVDD18_RADDR	1.8V supply voltage	-0.3	1.98	V
VDDIO_DDR_DQ VDDIO_DDR_MCLK VDDIO_DDR_R VDDIO_DDR_CA AVDD15_POR	1.5V supply voltage	-0.3	1.575	V
DVDD18_VQPS	1.8V supply voltage	-0.3	1.98	V

3.2 Recommended Operating Range

Table 3-2 Recommended Operating Range

Symbol or Pin name	Description	Min.	Typ.	Max.	Unit
VCCK (DVDD_CORE) DVDD_DDR_TX DVDD_DDR_RX	0.87V supply voltage	0.826	0.87	0.914	V
DVDD18IO_TL DVDD18IO_LT DVDD18IO_LB DVDD18IO_BL DVDD18IO_RB DVDD18IO_RTC0 DVDD18IO_RTC1	1.8V supply voltage	1.71	1.8	1.89	V
DVDD33IO_LB DVDD33IO_BL DVDD33IO_RB DVDD33IO_RTC0 DVDD33IO_RTC1	3.3V supply voltage	3.135	3.3	3.465	V
AVDD33_USB AVDD33_LD_P0	3.3V supply voltage	3.135	3.3	3.465	V
AVDD12_CKSQ AVDD12_WBG	1.2V supply voltage	1.14	1.2	1.26	V
AVDD09_SGMII AVDD09_SGMII	0.9V supply voltage	0.855	0.9	0.945	V
AVDD18_SGMII AVDD18_SGMII AVDD18_COM AVDD18_POR AVDD18_AUXADC AVDD18_PLLGP AVDD18_CKSQ AVDD18_USB AVDD18_WBG AVDD18_RADDR	1.8V supply voltage	1.71	1.8	1.89	V
VDDIO_DDR_DQ VDDIO_DDR_MCLK VDDIO_DDR_R VDDIO_DDR_CA AVDD15_POR	1.5V supply voltage	1.425	1.5	1.575	V
DVDD18_VQPS	1.8V supply voltage	1.71	1.8	1.89	V

3.3 Thermal Characteristics

Thermal characteristics when stationary without an external heat sink in an air-conditioned environment.

Table 3-3 Thermal Characteristics

Symbol	Description	Performance	
		Typ	
TJ	Maximum Junction Temperature (Plastic Package)	125	°C
θJA	Junction to ambient temperature thermal resistance[1] for JEDEC 2L system PCB	23.65	°C/W
θJA	Junction to ambient temperature thermal resistance[1] for JEDEC 4L system PCB	18.05	°C/W
θJC	Junction to case temperature thermal resistance for JEDEC system PCB	8.05	°C/W
ψJt	Junction to the package thermal resistance for JEDEC 2L PCB	1.75	°C/W
ψJt	Junction to the package thermal resistance for JEDEC 4L PCB	1.15	°C/W

Note: JEDEC 51-9 system FR4 PCB size: 101.5 x 114.5 mm (4”x4.5”)

3.4 Current Consumption

Please reference to Application note.

3.5 Storage Conditions

The calculated shelf life in a sealed bag is 12 months if stored between 5 °C and 40 °C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

- Mounted within 168 hours of factory conditions, i.e. < 30 °C at 60% RH.
- Storage humidity needs to maintained at < 10% RH.
- Baking is necessary if the customer exposes the component to air for over 168 hrs, baking conditions: 125 °C for 8 hrs.

3.6 AC Electrical Characteristics

3.6.1 UART Interface

MT7981B utilizes the Universal Asynchronous Receiver Transmitter (UART) interface as its host control interface. The electrical timing characteristic for the UART interface is illustrated below.

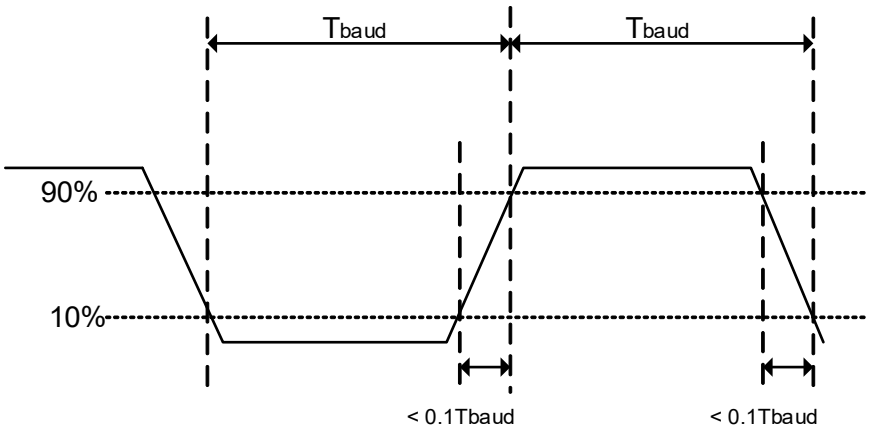

Figure 3-1 UART Timing

3.6.2 SPI Interface

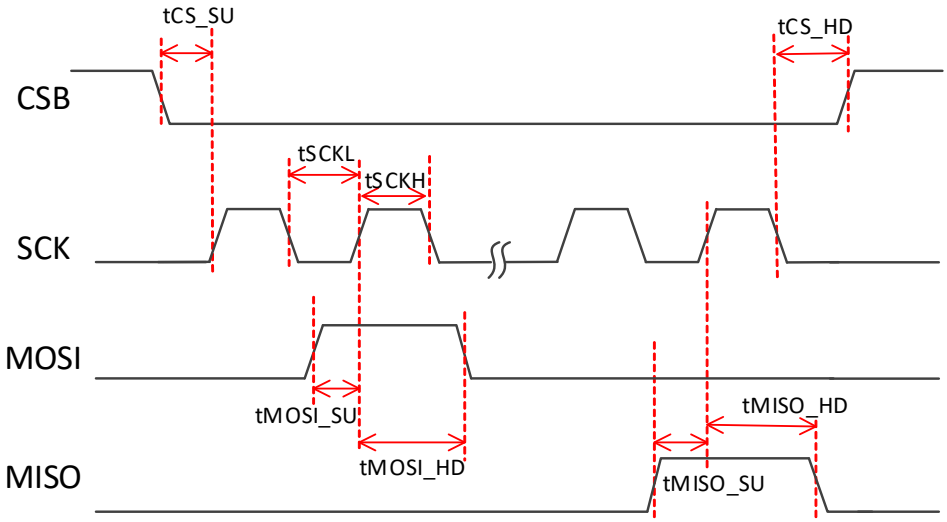

Figure 3-2 SPI Master Timing

Table 3-4 SPI Master Electrical Specifications

Symbol	Description	Performance			Units	Note
		Min.	Typ.	Max.		
fSCK	SPI Master SCK Clock frequency	-	-	52	MHz	
tMOSI_SU	MOSI to SCK Rising setup Time	6.6	-	-	ns	Tsck/2–Tskew-Tmargin
tMOSI_HD	SCK Rising to MOSI hold Time	6.6	-	-	ns	Tsck/2–Tskew-Tmargin
tSCKL	SCK Low Pulse	7.2	-	-	ns	Tsck/2*0.75
tSCKH	SCK High Pulse	7.2	-	-	ns	Tsck/2*0.75
tCSB_SU[1]	CSB Falling to SCK Rising Setup Time	1.8	-	-	ns	Tbclk–Tskew–Tmargin
tCSB_HD[1]	SCK Falling to CSB Rising Hold Time	1.8	-	-	ns	Tbclk–Tskew–Tmargin
tMISO_SU[2]	MISO to SCK Rising Setup Time requirement	0	-	-	ns	
tMISO_HD[3]	SCK Rising to MISO Hold Time requirement	0	-	-	ns	

Notes:

1. In CS GPIO mode, SPI_CS handled by SW. SW should pull down SPI_CS pin before SPI starts transferring and pull up SPI_CS pin when SPI completes the transaction. Based on the sequence above, the minimum specification of tCSB_SU and tCSB_HD time can be satisfied.
2. To achieve the min value of tMISO_SU, the internal sample clock delay of SPI master should be adjusted.
3. MISO data valid time should be one cycle of fSCK.
4. For dual mode or quad mode, all the output data pins can refer to the MOSI timing parameters, and all the input data pins can refer to the MISO timing parameters.

3.6.3 SPI NAND Flash Interface

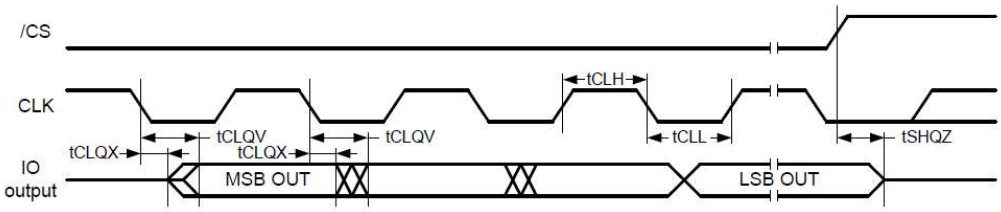

Figure 3-3 SPI NAND Serial Output Timing

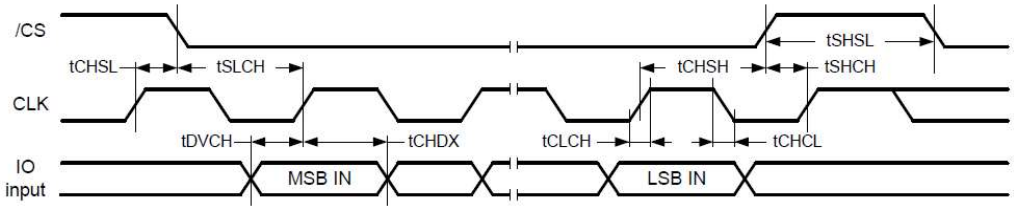

Figure 3-4 SPI NAND Serial Input Timing

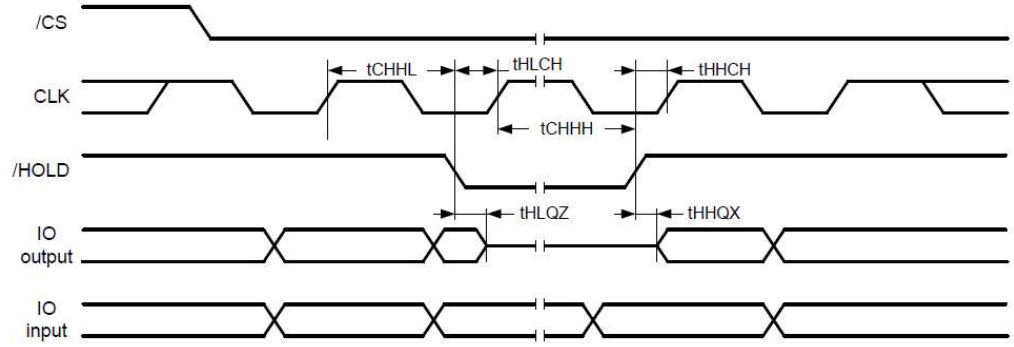

Figure 3-5 SPI NAND /HOLD Timing

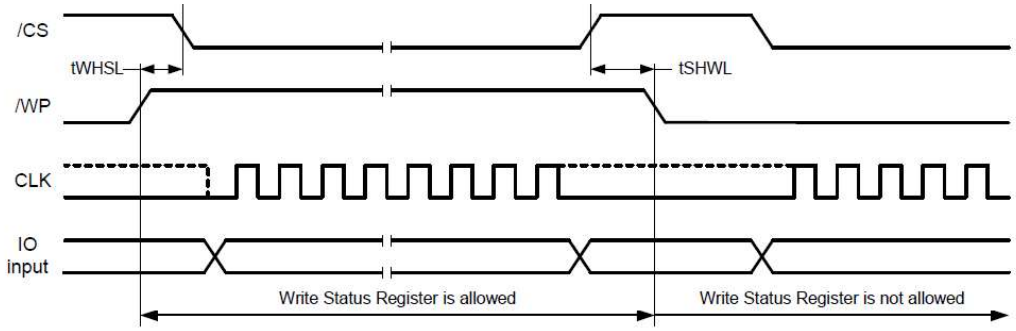

Figure 3-6 SPI NAND /WP Timing

Table 3-5 SPI NAND Interface Diagram Key

Symbol	Description	Min	Max	Unit
tCLH, tCLL,	Clock High, Low Time for all instructions	4	-	ns
tCLCH	Clock Rise Time peak to peak	0.1		V/ns
tCHCL	Clock Fall Time peak to peak	0.1		V/ns
tSLCH	/CS Active Setup Time relative to CLK	5		ns
tCLCH	/CS Not Active Hold Time relative to CLK	5		ns
tDVCH	Data in Setup Time	2		ns
tCHDX	Data in Hold Time	3		ns
tCHSH	/CS Active Hold Time relative to CLK	3		ns
tSHCH	/CS Not Active Setup Time relative to CLK	3		ns
tSHSL1	/CS Deselect Time(for Array Read → Array Read)	10		ns
tSHSL2	/CS Deselect Time(for Erase, Program or Read Status Registers → Read Status Registers)	50		ns
tSHQZ	Output Disable Time		7	ns

Symbol	Description	Min	Max	Unit
tCLQV	Clock Low to Output Valid		7	ns
tCLQX	Output Hold Time	2		ns
tHLCH	/HOLD Active Setup Time relative to CLK	5		ns
tCHHH	/HOLD Active Hold Time relative to CLK	5		ns
tHHCH	/HOLD Not Active Setup Time relative to CLK	5		ns
tCHHL	/HOLD Not Active Hold Time relative to CLK	5		ns
tHHQX	/HOLD to Output Low-Z		7	ns
tHLQZ	/HOLD to Output High-Z		12	ns
tWHSL	Write Protect Setup Time Before /CS Low	20		ns
tSHWL	Write Protect Hold Time After /CS High	100		ns
tW	Status Register Write Time		50	ns
tRST	/CS High to next Instruction after Reset during Page Data Read / Program Execute / Block Erase		5/10/500	ns
tRD1	Read Page Data Time (ECC disabled)		25	us
tRD2	Read Page Data Time (ECC enabled)		60	us

3.7 DC Characteristics

3.7.1 3.3V IO

Table 3-6 3.3V IO Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIL	Input low voltage	-0.30	-	0.83	V
VIH	Input high voltage	2.06	-	3.63	V
VOL	Output low voltage	-0.30	-	0.41	V
VOH	Output high voltage	2.48	-	3.63	V
RPU	Input pull-up resistance	10	50	100	KΩ
RPD	Input pull-down resistance	5	7.5	10	KΩ

3.7.2 1.8V IO

Table 3-7 1.8V IO Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIL	Input low voltage	-0.30	-	0.63	V
VIH	Input high voltage	1.17	-	2.10	V
VOL	Output low voltage	-	-	0.45	V
VOH	Output high voltage	1.35	-	-	V
RPU	Input pull-up resistance	40	75	190	KΩ
RPD	Input pull-down resistance	40	75	190	KΩ

3.8 Power on Sequence

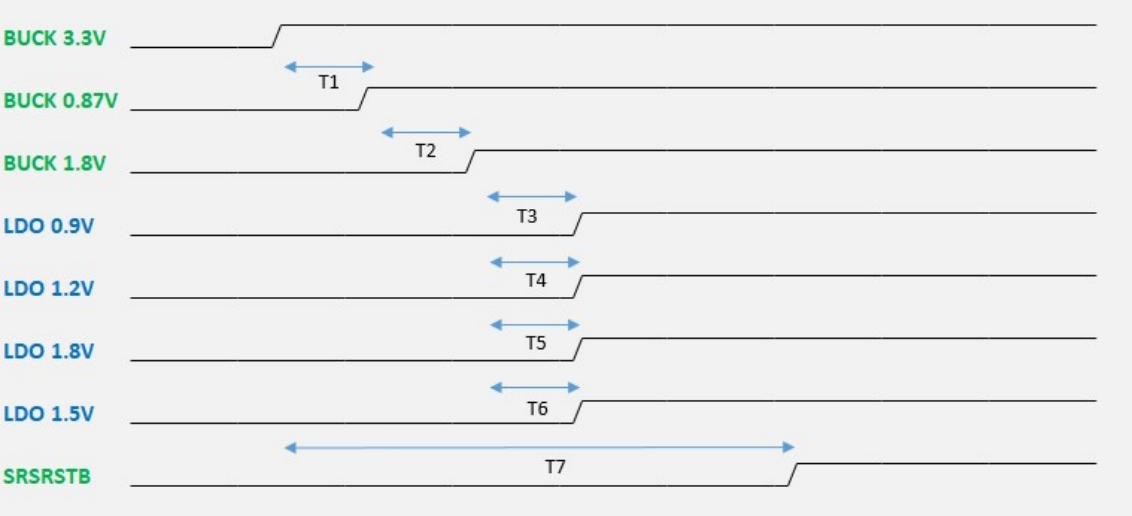

Figure 3-7 Power ON Sequence

Table 3-8 Power on sequence parameters

Symbol	Description	Min	Max	Unit
T1	BUCK_3.3V to BUCK_0.87V	0.5	5	ms
T2	BUCK_0.87V to BUCK_1.8V	0.5	5	ms
T3	BUCK_1.8V to LDO_0.9V	2	6	ms
T4	BUCK_1.8V to LDO_1.2V	2	6	ms
T5	BUCK_1.8V to LDO_1.8V	2	6	ms
T6	BUCK_1.8V to LDO_1.5V	2	6	ms
T7	BUCK_3.3V to SRSRSTB release	35	-	ms

4 Package Information

4.1 Dimensions – TFBGA (13.0 x 11.7 x 1.2 mm)

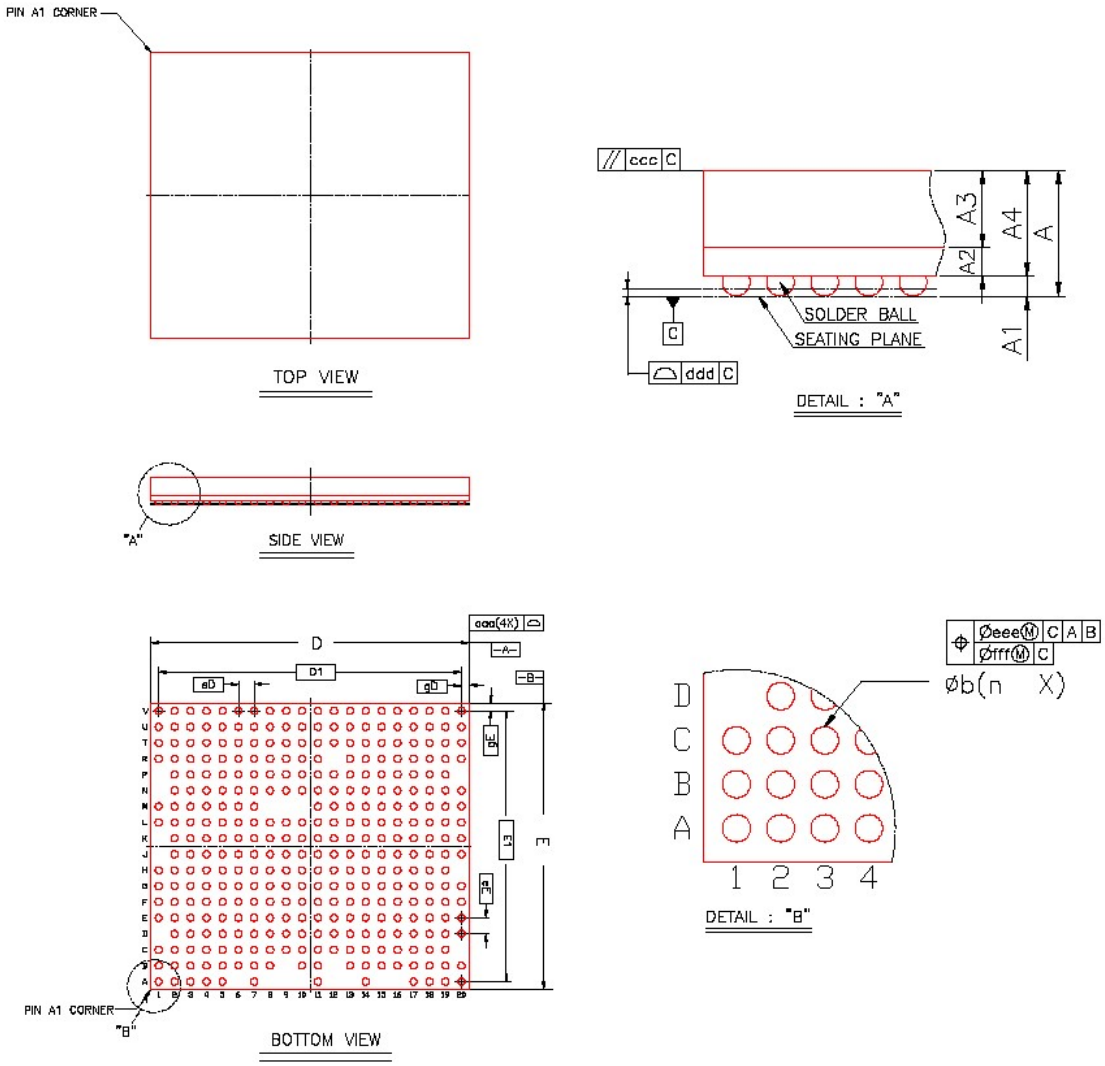

Figure 4-1 Package Dimension

NOTE:

1. Controlling dimensions are in millimeters.
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. The pattern of pin 1 fiducial is for reference only.

4.1.1 Diagram Key

Table 4-1 Package Diagram Key

Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			TFBGA		
Body Size	X	D	12.950	13.000	13.050
	Y	E	11.650	11.700	11.750
Ball Pitch	X	eD		0.650	
	Y	eE		0.650	
Mold Thickness		A3		0.700 Ref.	
Substrate Thickness		A2		0.210 Ref.	
Substrate+Mold Thickness		A4	0.850	0.910	0.970
Total Thickness		A	–	–	1.200
Ball Diameter				0.300	
Ball Stand Off		A1	0.160	0.210	0.260
Ball Width		b	0.250	0.300	0.350
Package Edge Tolerance		aaa		0.050	
Mold Flatness		ccc		0.100	
Coplanarity		ddd		0.080	
Ball Offset (Package)		eee		0.150	
Ball Offset (Ball)		fff		0.050	
Ball Count		n		338	
Edge Ball Center to Center	X	D1		12.350	
	Y	E1		11.050	
Edge Ball Center to Package Edge	X	gD		0.325	
	Y	gE		0.325	

4.2 Reflow Profile Guideline

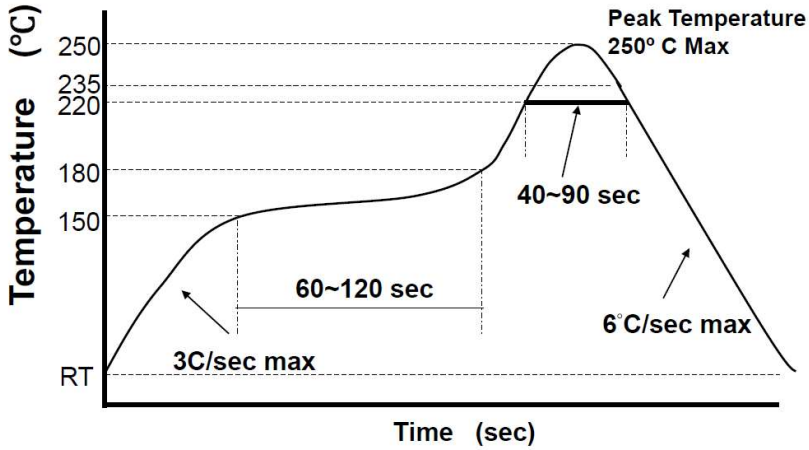

Figure 4-2 Reflow profile

Notes;
1.Reflow profile guideline is designed for SnAgCulead-free solder paste.
2.Reflow temperature is defined at the solder ball of package.
3.MTK would recommend customer following the solder paste vendor's guideline to design a profile appropriate your line and products.
4.Appropriate N_2 atmosphere is recommended since it would widen the process window and mitigate the risk for having solder open issues.

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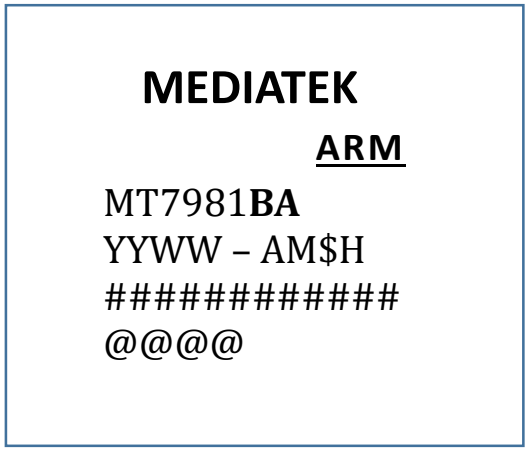
4.3 Top Marking



Description:

YYWW: Date code

#: LOT NO.

$/@: Internal control code

Figure 4-3 MT7981B Top marking

4.4 Ordering Information

Part Number	Temperature Range	Package (Green/RoHS Compliant)
MT7981BA	-10°C ~ 70°C	13.0 x 11.7 mm, TFBGA

Note: a heat sink is required in max ambient temperature.

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